S81	126	(clock adj1 speed) near4 ((arithmetic adj1 logic adj1 unit$1) or ALUs or (execution adj1 unit$1) or (process$3 adj1 unit$1))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/10/18 14:11
S82	4	(clock adj1 speed) near4 ((arithmetic adj1 logic adj1 unit$1) or ALUs or (execution adj1 unit$1) or (process$3 adj1 unit$1)) near4 ((high$2 or fast$2) and (low$3 or slow$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/04/13 14:31
S83	4	(clock adj1 speed) with ((arithmetic adj1 logic adj1 unit$1) or ALUs or (execution adj1 unit$1) or (process$3 adj1 unit$1)) with ((high$2 or fast$2) and (low$3 or slow$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/04/13 14:32
S84	50	(clock adj1 speed) same ((arithmetic adj1 logic adj1 unit$1) or ALUs or (execution adj1 unit$1) or (process$3 adj1 unit$1)) same ((high$2 or fast$2) and (low$3 or slow$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/10/18 15:39
S85	17	("5428754").URPN.	USPAT	OR	OFF	2005/04/13 14:39
S86	35	("3656123").URPN.	USPAT	OR	OFF	2005/04/13 14:40
S87	753	(712/23).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2005/10/18 14:10
S88	115	(712/30).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2005/10/18 14:10
S89	345	(712/221).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2005/10/18 14:10
S90	1094	(713/400).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2005/10/18 14:10
S91	665	(713/501).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2005/10/18 14:10

S92	845	(713/600).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2005/10/18 14:11
S93	416	((clock or cycle$1) adj1 (speed or tim$3)) near4 ((arithmetic adj1 logic adj1 unit$1) or ALUs or (execution adj1 unit$1) or (process$3 adj1 unit$1))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/10/18 14:11
S94	165	((clock or cycle$1) adj1 (speed or tim$3)) same ((arithmetic adj1 logic adj1 unit$1) or ALUs or (execution adj1 unit$1) or (process$3 adj1 unit$1)) same ((high$2 or fast$2) and (low$3 or slow$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/10/18 15:44

S12	0	compar$4 near4 ((ALU$1 or ($point adj1 unit$1)) adj1 result$1) near4 $3match$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/09/20 09:01
S13	1339	compar$4 adj1 result$1 near4 $3match$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/09/20 09:03
S14	399	(compar$4 adj1 result$1) near4 $3match$3 same (ALU$1 or (arithmetic adj2 unit$1) or process$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/09/20 09:04
S15	15	(compar$4 adj1 result$1) near4 $3match$3 same (ALU$1 or (arithmetic adj2 unit$1))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/09/20 09:07
S16	204	(compar$4 adj1 result$1) near4 (data near4 $3match$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/09/20 09:08
S17	6	(compar$4 adj1 result$1) near4 (data near4 $3match$3) near4 count$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/09/20 09:10
S18	6	(compar$4 adj1 output$1) near4 (data near4 $3match$3) near4 count$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/09/20 09:29
S19	310	(compar$4 near4 ((ALU$1 or arithmetic or process$3) output$1)) near4 $3match$3 near4 (count$3 or track$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/09/20 09:31
S20	292	(compar$4 near4 ((ALU$1 or arithmetic or process$3) output$1)) near4 $3match$3 near4 (count$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/09/20 09:31
S21	3	(compar$4 near4 ((ALU$1 or arithmetic or process$3) near4 output$1)) near4 $3match$3 near4 (count$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/09/20 09:32
S22	3	(compar$4 near4 ((ALU$1 or arithmetic or process$3) near4 output$1)) near4 $3match$3 near4 (count$3 or track$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/09/20 09:32
S23	81	(compar$4 near4 ((ALU$1 or arithmetic or process$3) near4 output$1)) near4 $3match$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/09/20 09:35

S24	3	(compar$4 near4 ((ALU$1 or arithmetic or process$3) near4 output$1)) near4 $3match$3 with (count$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/09/20 09:33
S25	11	(compar$4 near4 ((ALU$1 or arithmetic or process$3) near4 output$1)) near4 $3match$3 same (count$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/09/20 09:33
S26	9	(compar$4 near4 ((ALU$1 or arithmetic) near4 output$1)) near4 $3match$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/09/20 09:46
S27	0	compar$4 near4 ((floating adj1 point$1) near4 output$1) near4 $3match$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/09/20 09:46
S28	0	compar$4 near4 ((floating?point$1) near4 output$1) near4 $3match$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/09/20 09:47
S29	0	comparing near4 ((arithmetic or logic) adj1 (outputs or results)) near4 $3match$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/09/20 09:48
S30	223	comparing near4 (outputs or results) near4 $3match$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/09/20 09:48
S31	0	comparing near4 (data adj1 (outputs or results)) near4 $3match$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/09/20 09:48
S32	18	comparing near4 (data near4 (outputs or results)) near4 $3match$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/09/20 09:51
S33	40	comparator near4 (data near4 (outputs or results)) near4 $3match$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/09/20 09:51
S34	1	("6161171").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2004/08/10 15:52
S35	2	(("3656123") or ("5428754")).PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2004/08/10 09:04

S36	1	"20020038418"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/08/10 13:56
S37	14	(clock adj1 frequency) near4 ALU	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/08/10 13:57
S38	0	(long adj1 latency adj1 instruction$1) near4 (co?processor$1)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/08/10 16:17
S39	0	(long adj1 latency adj1 instruction$1) same (co?processor$1)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/08/10 16:04
S40	1	(long adj1 latency adj1 instruction$1) near4 separate	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/08/10 16:04
S41	100	long adj1 latency adj1 instruction$1	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/08/10 16:05
S42	39	load near4 co?processor$1	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/08/10 16:15
S43	606	memory near4 co?processor$1	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/08/10 16:17
S44	0	(long adj1 latency) near4 (co?processor$1)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/08/10 16:17
S45	58	memory adj1 co?processor$1	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/08/10 16:26
S46	8	I/O adj1 co?processor$1	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/08/10 16:26
S47	13703	I/O near4 processor$1	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/08/10 16:27

S48	2477	I/O adj1 processor$1	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/08/10 16:27
S49	84	I/O near4 co?processor$1	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/08/10 16:27
S50	8	I/O adj1 co?processor$1	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/08/10 16:29
S51	512	load adj1 store adj1 units	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/08/10 16:29
S52	12	(load adj1 store adj1 units) near4 processors	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/08/10 16:29
S53	0	(load adj1 store adj1 units) near4 (instruction adj1 length)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/08/10 16:32
S54	1	(load adj1 store adj1 units) same (instruction adj1 length)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/08/10 16:33
S55	2	(processing adj1 units) same (instruction adj1 length)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/08/11 09:44
S56	5	("3401376" | "3248708" | "3426328" | "3569939" | "3573743").PN.	USPAT	OR	OFF	2004/08/11 09:08
S57	35	"3656123".URPN.	USPAT	OR	OFF	2004/08/11 09:08
S58	0	((float$3 adj1 point) adj1 (units or co?processors or processors)) near4 (instruction near4 tim$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/08/11 09:46
S59	16	((float$3 adj1 point) adj1 (units or co?processors or processors)) near4 tim$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/08/11 09:52
S60	10	("4725973" | "5233694" | "5481736" | "5488729" | "5560035" | "5692139" | "5838986" | "5890009" | "5923871" | "6163837").PN.	USPAT	OR	OFF	2004/08/11 09:49

S61	217	(float$3 adj1 point) near4 instruction$1 near4 (length or tim$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/08/11 10:14
S62	88	(float$3 adj1 point) adj1 instruction$1 near4 (length or tim$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/08/12 08:24
S63	6	(integer and (floating adj1 point)) adj1 (unit$1 or processor$1 or co?processor$1) same (execut$3 adj1 tim$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/08/12 08:34
S64	143	(integer and (floating adj1 point)) adj1 (unit$1 or processor$1 or co?processor$1) same (instruction$1 adj1 execut$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/08/12 08:35
S65	3	(integer and (floating adj1 point)) adj1 (unit$1 or processor$1 or co?processor$1) same (clock near4 frequency)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/08/12 08:43
S66	55	(integer and (floating adj1 point)) adj1 (unit$1 or processor$1 or co?processor$1) same (clock near4 cycle$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/08/12 08:43
S67	55	(integer and (floating adj1 point)) adj1 (unit$1 or processor$1 or co?processor$1) same (clock$3 near4 cycle$1)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/08/12 08:43
S68	23	("4658355" | "5363495" | "5428807" | "5497499" | "5572690" | "5600848" | "5682493" | "5699460" | "5704054" | "5748936" | "5758139" | "5805838" | "5838939" | "5913059" | "5943491" | "5944816" | "5974524" | "5987588" | "6065109" | "6085316" | "6185668" | "6205538" | "6381692").PN.	USPAT	OR	OFF	2004/08/12 08:45
S69	728	(712/23).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2004/08/12 09:48
S70	109	(712/30).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2004/08/12 09:48

S71	292	(712/221).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2004/08/12 09:49
S72	872	(713/400).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2004/08/12 09:49
S73	594	(713/501).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2004/08/12 09:49
S74	664	(713/600).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2004/08/12 09:49
S75	744	(712/23).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2005/04/13 14:25
S76	112	(712/30).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2005/04/13 14:26
S77	330	(712/221).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2005/04/13 14:26
S78	1013	(713/400).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2005/04/13 14:26
S79	634	(713/501).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2005/04/13 14:26
S80	770	(713/600).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2005/04/13 14:27

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1	("6256745").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2004/09/20 08:36
S2	1	("5828868").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2004/09/20 08:52
S3	1	("6216234").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2004/09/20 08:53
S4	0	compar$4 near4 (ALUs near4 result$1) near4 $3match$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/09/20 08:53
S5	3086	compar$4 near4 result$1 near4 $3match$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/09/20 08:54
S6	1554	compar$4 adj2 result$1 near4 $3match$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/09/20 08:54
S7	3	compar$4 near4 ((ALU$1 or arithmetic) adj1 result$1) near4 $3match$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/09/20 08:55
S8	16	compar$4 near4 ((ALU$1 or arithmetic) near4 result$1) near4 $3match$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/09/20 08:56
S9	2128273	compar$4 adj$1 result$1 near4 $3match$3 near4 ALU$1	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/09/20 08:57
S10	1299	(compar$4 adj$1 result$1) near4 $3match$3 near4 (ALU$1 or unit$1)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/09/20 08:58
S11	44	(compar$4 adj1 result$1) near4 $3match$3 near4 (ALU$1 or unit$1)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/09/20 09:00

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#1	((((clock <or> cycle <or> cycles) <near/1> (speed <or> time <or> timing <or> times)) <paragraph> ((arithmetic <near/1> logic) <or> alu <or> alus <or> (execution <near/1> (unit <or> units)) <or> ((process <or> processing) <near/1> (unit <or> units))) <paragraph> ((high <or> higher <or> fast <or> faster) <and> (low <or> lower <or> slow <or> slower)))<in>metadata)	1(
#2	((((clock <or> cycle) <sentence> speed) <paragraph> ((instruction <or> instructions) <sentence> (execution <or> executing <or> process <or> processing)))<in>metadata)	3(

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A High Speed Dataflow Processing Element and its ... - by Coleman - 4 citations
Operating Systems - by Stallings - 256 citations
A Dynamic Instruction Set Computer - by Wirthlin - 146 citations

Apple - PowerPC G5 - **Execution** Core
... up to eight **instructions** per **clock cycle** are fetched, decoded and divided ...
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Instead of one **instruction** being in the processor (central **processing** unit, ...
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MacTRACK | Advanced **Instruction Processing**
In the Intel world particularly, **instructions** are complex to **process**, ...
Imagine a processor which can **execute** 10 **instructions** on a **clock cycle** with a ...
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The Infinity Machine
If this "infinity" **instruction** can turn a 1KHz **clock cycle** into an infinite ...
execute instructions until the **process** reaches a blocking system call. ...
www.chiark.greenend.org.uk/~sgtatham/infinity.html - 34k - Cached - Similar pages

PC World | HTML Developer's Guide | CPUs
The **execution** of an **instruction** requires many separate steps -- fetching and ...
Clock Cycle Speed. In order to correctly synchronise the actions of a CPU, ...
www.pcworld.idg.com.au/index.php/ id;1641589960;pp;2;taxid;115 - Similar pages

Central **processing** unit - Wikipedia, the free encyclopedia
After the **execution** of the **instruction**, the entire **process** repeats, with the next **instruction cycle** normally fetching next-in-sequence **instruction** due to ...
en.wikipedia.org/wiki/Central_**processing**_unit - 57k - Oct 17, 2005 - Cached - Similar pages

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characterizes processor signal **processing execution speed**. ... **clock speed** of 300 MHz and executes up to eight **instructions** per **clock cycle**. This gives ...
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The Pentium 4 and the G4e: an Architectural Comparison: Part I ...
Since each stage always lasts exactly one **clock cycle**, shorter pipeline stages ... The P4 can have up to 126 **instructions** in various stages of **execution** ...
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A High **Speed** Dataflow **Processing** Element and its Performance Compared to a von Neumann Mainframe
JN Coleman - IPPS, 1993 - ieeexplore.ieee.org
... therefore opted to use a very high **speed** main memory ... memory has an access time of two **clock** periods, and ... maintain an **execution** rate of one **cycle** per **instruction** ...
Cited by 4 - Web Search - ieeexplore.ieee.org

[BOOK] Operating Systems
W Stallings, H Deitel, ANI TO - 2004 - cs.newcastle.edu.au
... The **clock** generator sets the cadence for the ... code which takes too long –**SPEED** THINGS UP! ... **Instruction cycle** Fetch –Program Counter • used as a pointer to ...
Cited by 256 - View as HTML - Web Search - all 2 versions » - Library Search

A Dynamic **Instruction** Set Computer
MJ Wirthlin, BL Hutchings, UT Provo - IEEE Symposium on FPGAs for Custom Computing Machines, 1995 - doi.ieeecomputersociety.org
... function in a single **clock cycle**, such as basic arith- metic ... a match against its own opcode during the OF **cycle**. ... bits and operates at the host bus **speed** of 7.5 ...
Cited by 146 - Web Search - doi.ieeecs.org - splish.ee.byu.edu - portal.acm.org - all 9 versions »

The digital signal processor Derby
J Eyre, BDT Inc - IEEE Spectrum, 2001 - spectrum.ieee.org
... to parallelism Issuing multiple **instructions** per **cycle** is one ... to run at a high **clock speed** without requiring ... that used caches had only **instruction** caches, not ...
Cited by 28 - Web Search - dx.doi.org - ieeexplore.ieee.org - portal.acm.org - all 5 versions »

... Array Cellular Logic Processors for Single-**Instruction** Multiple-Data Parallel-Pipeline **Processing**
JM Wu, CB Kuznia, B Hoanca, CH Chen, AA Sawchuk - Appl. Opt, 1999 - ao.osa.org
... has no IO bottleneck, the **processing speed** scales linearly ... blocks in 2D parallel in a single **clock cycle**. ... operation and therefore the fewest **clock** cycles of ...
Cited by 13 - Web Search - my.com.nthu.edu.tw - mail.com.nthu.edu.tw - adsabs.harvard.edu - all 7 versions »

Code positioning to reduce **instruction** cache misses in signal **processing** applications on multimedia ...
HJ Stolberg, M Ikekawa, I Kuroda - ... Conference on Acoustics, Speech and Signal **Processing** - ieeexplore.ieee.org
... which in turn account for high processor **clock speed**. ... as well as direct-mapped **instruction** and data ... always be accomplished within one **clock cycle**, external me ...
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COMPILED HW/SW CO-SIMULATION
V Zivojnovik, H Meyr - ieeexplore.ieee.org
... environment is able to deliver fast, **clock**-accurate simulation. ... which is executed in the current **cycle**, or in ... of the hardware simulator and thereby the **speed**. ...
Cited by 35 - Web Search - ieeexplore.ieee.org - portal.acm.org

A Reconfigurable Architecture for High **Speed** Computation by Pipeline **Processing**
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... application, the number of **instructions** that can ... while supporting the maximum **instruction** level parallelism ... this architecture, high **clock cycle speed** and small ...
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